GLSVLSI 2016 Schedule

	Wednesday, May 18		**Thursday, May 19**		**Friday, May 20**	
8:00 – 8:30	Speakers' Breakfast (*Room 906*)		Speakers' Breakfast (*Room 906*)		Speakers' Breakfast (*Room 906*)	
8:30 – 9:00	Opening session (*Room 206*)					
9:00 – 10:00	Keynote 1: (*Room 206*) *Marc Witteman, Riscure*		Keynote 2: (*Room 206*) *Prof. Yusuf Leblebici, EPFL*		Keynote 4: (*Room 206*) *Prof. Ingrid Verbauwhede, KU Leuven*	
10:00 – 10:30	Coffee break		Coffee break		Coffee break	
10:30 – 12:00	Session 1 (*Room 210*) VLSI circuits 1 **39*, 67**, 221, 173	Session 2 (*Room 211*) VLSI and Test **117, 186,** 189, 85	Session 6 (*Room 210*) Test 2 **166, 113**, 47, 103	Special Session 2 (*Room 211*) Creating Circuits with Living Systems Using Synthetic Biology	Session 10 (*Room 210*) VLSI Design 2 **25, 128,** 32, 137	Special Session 4 (*Room 211*) Emerging Frontiers in Hardware Security
12:00 – 12:30	Lunch (*Room 906*)		Lunch & Keynote 3: (*Room 906*) *Prof. Kevin Fu, University of Michigan*		***Poster Session 2*** & Lunch (*Room 906*) *Low power: 21, 9, 100, 38* *Test: 254, 58, 96, 248* *Emerging: 82, 12, 206*	
12:30 – 1:00						
1:00 – 1:15	Session 3 (*Room 210*) VLSI Design 1 **182, 197*,** 60, 116	Session 4 (*Room 211*) CAD 1 **70*, 11**, 127, 35				
1:15 – 1:30					Session 11 (*Room 210*) Emerging 2 **14, 126,** 115, 185	Session 12 (*Room 211*) Low power 2 **92, 95**, 157, 183
1:30 – 2:30			Session 7 (*Room 210*) VLSI Circuits 2 **158**, 43, 77, 223, 74	Session 8 (*Room 211*) Emerging 1 **139***, 98, 102, 246		
2:30 – 2:45	***Poster Session 1*** & Coffee Break (*Atrium Outside Room 206*) *VLSI-D: 89, 170, 27, 239* *VLSI Cir: 168, 222, 255* *CAD: 202, 228, 229*					
2:45 – 3:00					Closing Remarks	
3:00 – 3:30			Coffee Break		**All rooms are located in ECE Department/Photonics Center at 8 St. Mary's Street.*	
3:30 – 5:00	Session 5 (*Room 210*) **Low power 1** **51, 97,** 23, 64	Special Session 1 (*Room 211*) IoT Security: Issues, Innovations and Interplays	Session 9 (*Room 210*) CAD 2 **62,** 249, 121, 133, 196	Special Session 3 (*Room 211*) Emerging Technology Devices and Security		
5:00 – 5:30	Steering Committee Meeting (*Room 339*)					
5:30 – 6:00			5:15 – Social Activity			
	6:15 - Welcome Reception					
			6:45 – Conference Banquet			

** Papers marked with stars are **best paper candidates**.*
*Numbers above represent the paper IDs. **Bolded** numbers demonstrate long presentations. SP demonstrates a special session paper.*

Wednesday, May 18		
8:00 – 8:30	Speakers' Breakfast (*Room 906*)	
8:30 – 9:00	Opening Session (*Room 206*)	
9:00 - 10:00	**Keynote 1: *Why Is It So Hard to Make Secure Chips?*** (*Room 206*) *Marc Witteman, Chief Executive Officer, Riscure, The Netherlands* (Chair: Ayse Coskun, Boston University)	
10:00 – 10:30	Coffee break	
10:30 - 12:00	Session 1 VLSI circuits 1 (*Room 210*) Chairs: Zain Navabi (Worcester Polytechnic Institute) Swaroop Ghosh (University of South Florida) **39* (L)** Chaohui Du, Guoqiang Bai and Xingjun Wu. High-Speed Polynomial Multiplier Architecture for Ring-LWE Based Public Key Cryptosystems **67 (L)** Kyle Juretus and Ioannis Savidis. Reduced Overhead Gate Level Logic Encryption 221 (S) Salin Junsangsri, Jie Han and Fabrizio Lombardi. A Design of a Non-Volatile PMC-Based (Programmable Metallization Cell) Register File 173 (S) Xiaolin Xu and Daniel Holcomb. A Clockless Sequential PUF with Autonomous Majority Voting	Session 2 VLSI and Test (*Room 211*) Chair: Weikang Qian (Shanghai Jiaotong University) **117 (L)** Bo Yuan, Yanzhi Wang and Zhongfeng Wang. Area-Efficient Error-Resilient Discrete Fourier Transformation Design using Stochastic Computing **186 (L)** Pei Luo, Cheng Li and Yunsi Fei. Concurrent Error Detection for Reliable SHA-3 Design 189 (S) Travis Boraten, Dominic DiTomaso and Avinash Kodi. Secure Model Checkers for Network-on-Chip (NoC) Architectures 85 (S) Sita Kondamadugula and Srinath R Naidu. Parameter-importance based Monte-Carlo Technique for Variation-aware Analog Yield Optimization
12:00 - 1:00	Lunch (*Room 906*)	
1:00 – 2:30	Session 3 VLSI Design 1 (*Room 210*) Chair: Himanshu Thapliyal (University of Kentucky) Houman Homayoun (George Mason University) **182 (L)** Amey Kulkarni, Tahmid Abtahi, Emily Smith and Tinoosh Mohsenin. Low Energy Sketching Engines on Many-Core Platform for Big Data Acceleration **197* (L)** Adam Page, Nasrin Attaran, Colin Shea, Houman Homayoun and Tinoosh Mohsenin. Low-Power ManyCore Accelerator for Personalized Biomedical Applications 60 (S) Jaya Dofe, Qiaoyan Yu, Hailang Wang, and Emre Salman. Hardware Security Threats and Potential Countermeasures in Emerging 3D ICs 116 (S) Qin Xiong, Zhonghai Lu, Fei Wu and Changsheng Xie. Real-Time Analysis for Wormhole NoC: Revisited and Revised	Session 4 CAD 1 (*Room 211*) Chair: Tosiron Adegbija (University of Arizona) Marisa López-Vallejo (Universidad Politécnica de Madrid) **70* (L)** Yu-Hsiang Hung, Sheng-Hsin Fang, Hung-Ming Chen, Shen-Min Chen, Chang-Tzu Lin and Chia-Hsin Lee. A New Methodology for Noise Sensor Placement Based on Association Rule Mining **11 (L)** Xiaotao Jia, Yici Cai, Qiang Zhou and Bei Yu. MCFRoute 2.0: A Redundant Via Insertion Enhanced Concurrent Detailed Router 127 (S) Fubing Mao, Wei Zhang, Bo Feng, Bingsheng He and Yuchun Ma. Modular Placement for Interposer based Multi-FPGA Systems 35 (S) Zhezhao Xu, Wenjian Yu, Chao Zhang, Bolong Zhang, Meijuan Lu and Michael Mascagni. A Parallel Random Walk Solver for the Capacitance Calculation Problem in Touchscreen Design

<table>
<tr><td>2:30 – 3:30</td><td colspan="2">Poster session 1 & Coffee Break (Atrium Outside Room 206)
Chair: Tali Moreshet (Boston University)
VLSI Design:
89 - Chen Yang, Yan Li, Wei Zhong and Song Chen. Real-Time Hardware Stereo Matching Using Guided Image Filter
170 - Yin Liu and Keshab K. Parhi. Computing Complex Functions using Factorization in Unipolar Stochastic Logic
27 - Mohsen Imani, Shruti Patil and Tajana Rosing. DCC: Double Capacity Cache for Narrow-Width Data Values
239 - Nidhi Batra, Pawan Sehgal, Shashwat Kaushik, Mohammad S. Hashmi, Sudesh Bhalla and Anuj Grover. Static Noise Margin based Yield Modelling of 6T SRAM for Area and Minimum Operating Voltage Improvement using Recovery Techniques
VLSI Circuits:
168 - Aditya Dalakoti, Carrie Segal, Merritt Miller and Forrest Brewer. Asynchronous High Speed Serial Links Analysis using Integrated Charge for Event Detection
222 - Wei Wei, Kazuteru Namba and Fabrizio Lombardi. Design and Comparative Evaluation of a Hybrid Cache Memory at Architectural Level
255 - Daniel Prashanth and Hae-Seung Lee. A Sampling Clock Skew Correction Technique for Time-Interleaved SAR ADCs
CAD:
202 - Xueyan Wang, Xiaotao Jia, Qiang Zhou, Yici Cai, Jianlei Yang, Mingze Gao and Gang Qu. Secure and Low-Overhead Circuit Obfuscation Technique with Multiplexers
228 - Md Farhadur Reza, Dan Zhao and Hongyi Wu. Task-Resource Co-allocation For Hotspot Minimization in Many-core NoCs
229 - Hamed Tabkhi, Majid Sabbagh and Gunar Schirner. Guiding Power/Quality Exploration for Communication-Intense Stream Processing</td></tr>
<tr><td>3:30 –5:00</td><td>Session 5 Low power 1 (Room 210)
Chair: Ioannis Savidis (Drexel University)
51(L) Valerio Tenace, Andrea Calimera, Enrico Macii and Massimo Poncino. Graphene-PLA (GPLA): a Compact and Ultra-Low Power Logic Array Architecture
97 (L) Govinda Sannena and Bishnu Prasad Das. A Metastability Immune Timing Error Masking Flip-Flop for Dynamic Variation Tolerance
23 (S) Tosiron Adegbija. Exploring Configurable Non-Volatile Memory-based Caches for Energy-Efficient Embedded Systems
64 (S) Jaeyoung Park and Michael Orshansky. Multiple Attempt Write Strategy for Low Energy STT-RAM</td><td>Special Session 1 (Room 211)
IoT Security: Issues, Innovations and Interplays
Chair: Swarup Bhunia (University of Florida)
Speakers: Gang Qu (University of Maryland), Saverio Fazzari (Booz Allen Hamilton), Garrett Rose (University of Tennessee), Jia Di (University of Arkansas)
(SP1) Md Tanvir Arafin and Gang Qu. Secret Sharing and Multi-user Authentication: From Visual Cryptography to RRAM Circuits
(SP2) Douglas Palmer, Saverio Fazzari and Scott Wartenberg. Defense Systems and IoT: Security Issues in an Era of Distributed Command and Control
(SP3) Garrett S. Rose. Security Meets Nanoelectronics for Internet of Things Applications
(SP4) Thao Le, Jia Di, Mark Tehranipoor, Domenic Forte and Lei Wang. Tracking Data Flow at Gate-Level through Structural Checking</td></tr>
<tr><td>5:00 – 6:00</td><td colspan="2">Steering Committee Meeting (Room 339)</td></tr>
<tr><td>6:15 – 7:45</td><td colspan="2">Welcome Reception at the Boston University Castle
225 Bay State Road, Boston</td></tr>
<tr><td colspan="3">Thursday, May 19</td></tr>
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8:00 – 9:00	Speakers' Breakfast (*Room 906*)	
9:00 – 10:00	**Keynote 2: *Design and Implementation of Real-Time Multi-sensor Vision Systems*** (*Room 206*) *Prof. Yusuf Leblebici, EPFL, Switzerland* (Chair: Jie Han, University of Alberta)	
10:00 – 10:30	Coffee Break	
10:30 – 12:00	Session 6 Test 2 (*Room 210*) Chair: Qiaoyan Yu (University of New Hampshire) **166 (L)** Xijing Han, Marco Donato, Iris Bahar, Alexander Zaslavsky and William Patterson. Design of Error-Resilient Logic Gates with Reinforcement Using Implications **113 (L)** Sparsh Mittal and Jeffrey Vetter. Reducing Soft-error Vulnerability of Caches using Data Compression 47 (S) Song Bian, Michihiro Shintani, Shumpei Morita, Hiromitsu Awano, Masayuki Hiromoto and Takashi Sato. Workload-Aware Worst Path Analysis of Processor-Scale NBTI Degradation 103 (S) Ralph Nyberg, Johann Heyszl, Dietmar Heinz and Georg Sigl. Enhancing Fault Emulation of Transient Faults by Separating Combinational and Sequential Fault Propagation	Special Session 2 (*Room 211*) Creating Circuits with Living Systems Using Synthetic Biology Chair: Douglas Densmore (Boston University) *Speakers:* *Jacob Beal (BBN),* Engineering Complex Behaviors in Biological Organisms *Alec Nielsen (MIT),* Genetic Circuit Design Automation *Jonathan Babb (MIT),* Programmable Organoids for Drug Development
12:00 – 1:30	Lunch & **Keynote 3: *Medical Device Security: The First 165 Years*** (*Room 906*) *Prof. Kevin Fu, University of Michigan Ann Arbor, USA* (Chair: Martin Margala, University of Massachusetts Lowell)	
1:30 – 3:00	Session 7 VLSI Circuits 2 (*Room 210*) Chair: Hai Li (University of Pittsburgh) **158 (L)** Yongsuk Choi and Yong-Bin Kim. A Novel On-Chip Impedance Calibration Method for LPDDR4 Interface between DRAM and AP/SoC 43 (S) Rui Zhou and Weikang Qian. A General Sign Bit Error Correction Scheme for Approximate Adders 77 (S) Amr M. S. Tosson Abdelwahed, Mohab Anis and Lan Wei. RRAM Refresh Circuit: A Proposed Solution To Resolve The Soft-Error Failures For HfO_2/Hf 1T1R RRAM Memory Cell 223 (S) Ravi Patel, Kan Xu, Eby G. Friedman and Praveen Raghavan. Exploratory Power Noise Models of Standard Cell 14, 10, and 7 nm FinFET ICs 74 (S) Amr M. S. Tosson Abdelwahed, Adam Neale, Mohab Anis and Lan Wei. 8T1R: A Novel Low-power High-speed RRAM-based Non-volatile SRAM Design	Session 8 Emerging 1 (*Room 211*) Chair: Bo Yuan (City University of New York) **139* (L)** Naman Saraf and Kia Bazargan. Polynomial Arithmetic Using Sequential Stochastic Logic 98 (S) Yu Bai, Bo Hu, Weidong Kuang and Mingjie Lin. Ultra-Robust Null Convention Logic Circuit with Emerging Domain Wall Devices 102 (S) Ioannis A. Papistas and Vasilis F. Pavlidis. Inter-Tier Crosstalk Noise On Power Delivery Networks for 3-D ICs with Inductively-Coupled Interconnects 246 (S) Subrata Das, Soma Das, Adrija Majumder, Parthasarathi Dasgupta and Debesh Kumar Das. Delay Estimates for Graphene Nanoribbons: A Novel Measure of Fidelity and Experiments with Global Routing Trees
3:00 – 3:30	Coffee Break	

3:30 – 5:00	Session 9 CAD 2 (*Room 210*) Chair: Miroslav Velev (Aries Design Automation) **62 (L)** Pietro Mercati, Francesco Paterna, Andrea Bartolini, Mohsen Imani, Luca Benini and Tajana Simunic Rosing. VarDroid: Online Variability Emulation in Android/Linux Platforms 249 (S) Ning Liu, Caiwen Ding, Yanzhi Wang and Jingtong Hu. Neural Network-based Prediction Algorithms for In-Door Multi-Source Energy Harvesting System for Non-Volatile Processors 121 (S) Sara Vinco, Yukai Chen, Enrico Macii and Massimo Poncino. A Unified Model of Power Sources for the Simulation of Electrical Energy Systems 133 (S) Munish Jassi, Uzair Sharif, Daniel Müller-Gritschneder and Ulf Schlichtmann. Hardware-Accelerated Software Library Drivers Generation for IP-Centric SoC Designs 196 (S) Vincent Mirian and Paul Chow. Extracting Designs of Secure IPs using FPGA CAD Tools	Special Session 3 (*Room 211*) Emerging Technology Devices and Security Chair: JV Rajendran (UT Dallas) (SP5) Robert Karam, Rui Liu, Pai-Yu Chen, Shimeng Yu, Swarup Bhunia. Security Primitive Design with Nanoscale Devices: A Case Study with Resistive RAM (SP6) Yu Bi, X. Sharon Hu, Yier Jin, Michael Niemier, Kaveh Shamsi, Xunzhao Yin. Enhancing Hardware Security with Emerging Transistor Technologies (SP7) Chaofei Yang, Beiye Liu, Yandan Wang, Yiran Chen, Hai Li, Xian Zhang, Guangyu Sun. The Applications of NVM Technology in Hardware Security (SP8) Ilia A. Bautista Adames, Jayita Das, Sanjukta Bhanja. Survey of Emerging Technology Based Physical Unclonable Functions
5:15 – 6:45	**Social Activity:** Historic Boston Duck Tour *Meeting Location: Granby Street, between Bay State Rd. and Commonwealth Ave.* *(Tour buses will drop off at the banquet)*	
6:45 – 9:00	Light Reception followed by **Conference Banquet** at the Boston University Trustees Ballroom *1 Silber Way, Boston, 9th floor* (**Best paper award will be announced during dinner)*	

<table>
<tr><th colspan="3">Friday, May 20</th></tr>
<tr><td>8:00 – 9:00</td><td colspan="2">Speakers' Breakfast (Room 906)</td></tr>
<tr><td>9:00 – 10:00</td><td colspan="2">Keynote 4: VLSI Design Methods for Low Power Embedded Encryption (Room 206)
Prof. Ingrid Verbauwhede, KU Leuven, Belgium (Chair: Laleh Behjat, University of Calgary)</td></tr>
<tr><td>10:00 – 10:30</td><td colspan="2">Coffee break</td></tr>
<tr><td>10:30 – 12:00</td><td>Session 10 VLSI Design 2 (Room 210)
Chair: Brett Meyer (McGill University)
25 (L) Yong Chen, Emil Matus and Gerhard Fettweis. Trellis-search based Dynamic Multi-Path Connection Allocation for TDM-NoCs
128 (L) Morteza Soltani, Mohammad Ebrahimi and Zainalabedin Navabi. Prolonging Lifetime of Non-volatile Last Level Caches with Cluster Mapping
32 (S) Anastasios Psarras, Junghee Lee, Pavlos Mattheakis, Chrysostomos Nicopoulos and Giorgos Dimitrakopoulos. A Low-Power Network-on-Chip Architecture for Tile-based Chip Multi-Processors
137 (S) Marcelo Ruaro and Fernando Gehm Moraes. Dynamic Real-Time Scheduler for Large-Scale MPSoCs</td><td>Special Session 4 (Room 211)
Emerging Frontiers in Hardware Security
Chair: Ajay Joshi (Boston University) and Gang Qu (University of Maryland)
Speakers: Yuan Xie (UCSB), Ruby Lee (Princeton), Yan Solihin (NSF), Yaw Obeng (NIST), Sukarno Mertoguno (ONR), Lisa Mcilrath (Raytheon BBN)
(SP9) Peng Gu, Shuangchen Li, Dylan Stow, Russell Barnes, Liu Liu, Eren Kursun, Yuan Xie. Leveraging 3D Technologies for Hardware Security: Opportunities and Challenges</td></tr>
<tr><td>12:00 – 1:15</td><td colspan="2">Poster Session 2 & Lunch (Room 906)
Chair: Hamed Tabkhi (Northeastern University)
Low power:
21 - Jiachen Song, Xi Li, Beilei Sun, Zhinan Cheng, Chao Wang and Xuehai Zhou. FCM: Towards Fine-Grained GPU Power Management for Closed Source Mobile Games
9 - Mohamad Hammam Alsafrjalani and Ann Gordon-Ross. Quality of Service-Aware, Scalable Cache Tuning Algorithm in Consumer-based Embedded Devices
100 - Saman Kiamehr, Mojtaba Ebrahimi and Mehdi B. Tahoori. Temperature-aware Dynamic Voltage Scaling for Near-Threshold Computing
38 - Tuhin Subhra Chakraborty, Santanu Kundu, Deepak Agrawal, Sanjay Tanaji Shinde, Jacob Mathews and Rekha K. James. Leakage Power Minimization in Deep Sub-Micron Technology by Exploiting Positive Slacks of Dependent Paths
Test:
254 - Adam Watkins and Spyros Tragoudas. An Enhanced Analytical Electrical Masking Model for Multiple Event Transients
58 - Dimitrios Stamoulis, Simone Corbetta, Dimitrios Rodopoulos, Pieter Weckx, Peter Debacker, Brett H. Meyer, Ben Kaczer, Praveen Raghavan, Dimitrios Soudris, Francky Catthoor and Zeljko Zilic. Capturing True Workload Dependency of BTI-induced Degradation in CPU Components
96 - Vijeta Rathore, Vivek Chaturvedi and Thambipillai Srikanthan. Performance Constraint-Aware Task Mapping to Optimize Lifetime Reliability of Manycore Systems
248 - Jordi Pérez-Puigdemont and Francesc Moll. ASIC Implementation of An All-digital Self-adaptive PVTA Variation-aware Clock Generation System
Emerging Technologies:
82 - Deliang Fan. Ultra-Low Energy Reconfigurable Spintronic Threshold Logic Gate
12 - Hang Zhang, Xuhao Chen, Nong Xiao, Fang Liu and Zhiguang Chen. Red-Shield: Shielding Read Disturbance for STT-RAM Based Register files on GPUs
206 - Poorna Marthi, Sheikh Rufsan Reza, Nazir Hossain, Jean-Francois Millithaler, Martin Margala, Ignacio Iñiguez de la Torre, Javier Mateos, Tomas Gonzalez. Modeling and Study of Two-BDT-Nanostructure based Sequential Logic Circuits</td></tr>
</table>

1:15 – 2:45	Session 11 Emerging 2 (*Room 210*) Chair: Jianwen Dai (Intel) **14 (L)** Qingda Hu, Guangyu Sun, Jiwu Shu and Chao Zhang. Exploring Main Memory Design Based on Racetrack Memory Technology **126 (L)** Ali Alsuwaiyan and Kartik Mohanram. An Offline Frequent Value Encoding for Energy-Efficient MLC/TLC Non-volatile Memories, 115 (S) Rajendra Bishnoi, Fabian Oboril and Mehdi B. Tahoori. Low-Power Multi-Port Memory Architecture based on Spin Orbit Torque Magnetic Devices 185 (S) Hassan Afzali-Kusha, Alireza Shafaei and Massoud Pedram. Optimizing the Operating Voltage of Tunnel FET-Based SRAM Arrays Equipped with Read/Write Assist Circuitry	Session 12 Low power 2 (*Room 211*) Chair: Kyung Ki Kim (Daegu University) Bishnu Prasad Das (Indian Institute of Technology) **92 (L)** Daniele Jahier Pagliari, Enrico Macii and Massimo Poncino. Approximate Differential Encoding for Energy-Efficient Serial Communication **95 (L)** Yukai Chen, Sara Vinco, Enrico Macii and Massimo Poncino. Fast Thermal Simulation using SystemC/AMS 157 (S) Cosimo Aprile, Luca Baldassarre, Vipul Gupta, Juhwan Yoo, Mahsa Shoaran, Yusuf Leblebici and Volkan Cevher. Learning-Based Near-Optimal Area-Power Trade-offs in Hardware Design for Neural Signal Acquisition 183 (S) Divya Pathak, Mohammad H. Hajkazemi, Mohammad K. Tavana, Houman Homayoun and Ioannis Savidis. Load Balanced On-Chip Power Delivery for Average Current Demand
2:45 – 3:00	Closing Remarks (*Room 206*)	