GLSVLSI 2022

Conference and Exhibition, June 6-8, 2022, Orange County, CA, USA

http://www.glsvlsi.org/

Sponsored by ACM SIGDA

The 32nd edition of GLSVLSI will be held as an in-person conference. Original, unpublished papers describing research in the general areas of VLSI and hardware design are solicited. Please visit http://www.glsvlsi.org/ for more information.

In addition to the traditional topic areas of GLSVLSI listed below, papers are solicited for a special theme of **"Machine learning in CAD, EDA, and VLSI Design and Security"**.

Program Tracks:

- **VLSI Design:** ASIC and FPGA design, microprocessors/micro-architectures, embedded processors, analog/digital/mixed-signal systems, NoC, SoC, IoT, interconnects, memories, bio-inspired and neuromorphic circuits and systems, BioMEMs, lab-on-a-chip, biosensors, CAD tools for biology and biomedical systems, implantable and wearable devices.
- **VLSI Circuits and Power Aware Design:** analog/digital/mixed-signal circuits, RF and communication circuits, chaos/neural/fuzzy-logic circuits, high-speed/low-power circuits, temperature estimation/optimization, power estimation/optimization, machine-learning for design and optimization of analog/digital/mixed-signal circuits, clock and power network optimization through applied machine-learning.
- **Computer-Aided Design (CAD):** hardware/software co-design, high-level synthesis, logic synthesis, simulation and formal verification, layout, design for manufacturing, algorithms and complexity analysis, physical design (placement, route, CTS), static timing analysis, signal and power integrity, machine learning for CAD and EDA design.
- **Testing, Reliability, Fault-Tolerance:** digital/analog/mixed-signal testing, reliability, robustness, static/dynamic defect- and fault-recoverability, variation-aware design, learning-assisted testing.
- **Emerging Computing & Post-CMOS Technologies:** nanotechnology, quantum computing, approximate and stochastic computing, sensor and sensor networks, post CMOS VLSI.
- **Hardware Security:** trusted IC, IP protection, hardware security primitives, reverse engineering, hardware Trojans, side-channel analysis, CPS/IoT security, machine learning for HW security.
- **VLSI for Machine Learning and Artificial Intelligence:** hardware accelerators for machine learning, novel architectures for deep learning, brain-inspired computing, big data computing, reinforcement learning, cloud computing for Internet-of-Things (IoT) devices.
- **Microelectronic Systems Education:** Pedagogical innovations using a wide range of technologies such as ASIC, FPGA, multicore, GPU, TPU, educational techniques including novel curricula and laboratories, assessment methods, distance learning, textbooks, and design projects, Industry and academic collaborative programs and teaching.

Paper submission deadline: ~~February 1, 2022~~ ~~February 15, 2022~~ **February 22, 2022 (11:59pm EST)**
Acceptance Notification: **March 21, 2022**
Camera-Ready: **April 5, 2022**

Paper Submission: Authors are invited to submit full-length (6 pages maximum), original, unpublished papers along with an abstract of at most 200 words. To enable blind review, the author list should be omitted from the main document. Previously published papers or papers currently under review for other conferences/journals should NOT be submitted and will not be considered. Electronic submission in PDF format to the **http://www.glsvlsi.org** website is required. Author and contact information (name, affiliation, mailing address, telephone, fax, e-mail) must be entered during the submission process.

Paper Format: Submissions should be in camera-ready two-column format, following the ACM proceedings specifications located at: **https://www.overleaf.com/latex/templates/association-for-computing-machinery-acm-sig-proceedings-template/bmvfhcdnxfty**
and the classification system detailed at: **http://www.acm.org/publications/class-2012**

Paper Publication and Presenter Registration: Papers will be accepted for regular or poster presentations at the symposium. Every accepted paper MUST have at least one author registered to the symposium by the time the camera-ready paper is submitted; at least one of the authors is also expected to attend the symposium and present the paper.